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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/692,957
Filing Date: October 24, 2003
Appellant(s): PANDE, ANAND

Michael T. Cruz
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 27 April 2007 appealing from the Office action mailed 05 May 2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is incorrect. A correct statement of the status of the claims is as follows:

The brief incorrectly states that claims 20 – 22 and 25 – 28 have been withdrawn without prejudice. However, only claims 20 – 22, 25, and 26 have been withdrawn without prejudice as claims 27 and 28 do not exist in the present application.

This appeal involves claims 1 – 19, 23, and 24.

Claims 20 – 22, 25, and 26 are withdrawn from consideration as not directed to the elected species.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

The following is a listing of the evidence relied upon in the rejection of claims under appeal:

6337893	Pontius	1-2002
6703950	Yi	3-2004
6810468	Miyamoto et al.	10-2004

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1 – 4, 12, 13, 16, and 23 – 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pontius (US Patent No. 6337893) in view of Yi (US Patent No. 6703950).

As per claim 1, Pontius teaches a first-in-first-out (FIFO) memory having a length of d where d is an integer (Pontius; Col 4 Lines 37 – 46). Pontius also teaches generating a code sequence having a length of 2d (Pontius; Col 4 Lines 37 – 46).

Pontius does not teach that the code sequence is a first code sequence and is generated from a second code sequence by removing one or more pairs of mirrored codes from the second code sequence. The first code sequence has a circular property and a Hamming length of one for any two consecutive codes of the first code sequence.

However, Yi teaches producing a code sequence of any even integer length and having a circular property and a Hamming length of one for any two consecutive codes by reducing a second code sequence (Yi; Figure 3a, Table 3a) into a first code sequence (Yi; Figure 3b, Table 3b) by removing one or more pairs of mirrored codes from the second code sequence (Yi; Figures 3a - 3b, Tables 3a - 3b, and Col 4 Lines 5 – 19).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings Pontius to include wherein the code sequence is generated by removing one or more pairs of mirrored codes from

a second code sequence to form a first code sequence that has a length of 2d, a circular property, and a Hamming length of one for any two consecutive codes because doing so allows for a geometrically reduced storage requirement (Yi; Col 2 Lines 54 – 58).

As per claim 2, Yi also teaches wherein the second code sequence has a circular property and a Hamming length of one for any two consecutive codes of the second code sequence (Yi; Figures 3a – 3b).

As per claim 3, Yi also teaches wherein the first code sequence is a Gray-code sequence (Yi; Figures 3a – 3b).

As per claim 4, Yi also teaches wherein the second code sequence is a Gray-code sequence (Yi; Figures 3a – 3b).

As per claim 12, Pontius and Yi also obviously teach wherein the FIFO memory comprises a write data input port and a read data input port because these ports are common on FIFO memory devices.

As per claim 13, Pontius and Yi also obviously teach wherein the FIFO memory comprises a write pointer input and a read pointer input because these inputs are common on FIFO memory devices.

As per claims 16 and 23, Pontius teaches a memory of depth d in which d is not equal to a value 2n and in which d and n are integers (Pontius; Col 4 Lines 37 – 46). A code sequence of length 2d is generated and used as read and write pointers to the memory (Pontius; Figure 1 Items 10 and 20, Col 4 Lines 37 – 46).

Pontius does not teach reducing a first Gray-code sequence of length 2n into a second Gray-code sequence of length 2d by removing one or more pairs of mirrored Gray-code sequences.

However, Yi teaches reducing a first Gray-code sequence of length 2n (Yi; Figure 3a, Table 3a) into a second Gray-code sequence of length 2d (Yi; Figure 3b, Table 3b) by removing one or more pairs of mirrored Gray-codes from the first Gray-code sequence (Yi; Figures 3a – 3b, Tables 3a – 3b, and Col 4 Lines 5 – 19).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Pontius to include wherein a Gray-code sequence of length 2n is reduced into a Gray-code sequence of 2d by removing one or more pairs of mirrored Gray-code sequences from the first Gray-code sequence because doing so allows for a geometrically reduced storage requirement (Yi; Col 2 Lines 54 – 58).

As per claim 24, Yi also teaches wherein at least one of the first code sequence and the second code sequence has at least one of a closed property and a Hamming distance of one (Yi; Figures 3a – 3b).

Claims 5 – 11, 14 – 15, and 17 – 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pontius (US Patent No. 6,337,893) in view of Yi (US Patent No. 6,703,950) and further in view of Miyamoto (US Patent No. 6,810,468).

As per claim 5, Pontius in combination with Yi teaches the data structure as described per claim 1 (see rejection of claim 1 above).

Pontius in combination with Yi does not teach that the code generator is coupled to a write pointer that is in turn connected to the first-in-first-out (FIFO) memory.

Miyamoto teaches an asynchronous FIFO memory that has a code generator connected to a write pointer (Miyamoto; Figure 1 Item 21).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Pontius in combination with Yi to include a write pointer that is connected to the code generator and the FIFO memory because doing so allows for determination of asynchronous FIFO status flags without stability errors.

As per claim 6, Miyamoto also teaches wherein the write pointer is coupled to the FIFO memory via at least one of a converter and a look-up table (Miyamoto; Figure 1 Item 21c).

As per claim 7, Miyamoto also teaches wherein the converter comprises a Gray-to-Binary converter (Miyamoto; Figure 1 Item 21c).

As per claim 8, Miyamoto also teaches wherein the code generator is coupled to a read pointer (Miyamoto; Figure 1 Item 22), which in turn is connected to the FIFO memory.

As per claim 9, Miyamoto also teaches wherein the read pointer is coupled to the FIFO memory via a Gray-to-binary converter (Miyamoto; Figure 1 Item 22c).

As per claim 10, Miyamoto also teaches wherein the code generator is coupled to a read pointer (Miyamoto; Figure 1 Item 22), which in turn, is coupled to the storage device.

As per claim 11, Pontius in combination with Yi and Miyamoto also obviously teaches wherein the storage device comprises a bank of registers because a bank of registers can store information the same way as a FIFO memory device.

As per claim 14, Pontius in combination with Yi and Miyamoto also obviously teaches that the asynchronous FIFO memory comprises a write clock domain and a read clock domain because asynchronous memory devices typically have a read clock domain and an independent write clock domain.

As per claim 15, Pontius in combination with Yi and Miyamoto also obviously teaches that the asynchronous FIFO memory comprises a write clock in the write clock domain, a read clock in the read clock domain, and that the read and write clock are asynchronous to each other because any asynchronous system has separate independent clocks to perform separate operations in different domains that are independently from one another.

As per claim 17, Miyamoto also teaches that reading and writing are asynchronous (Miyamoto; Col 3 Lines 34 – 37).

As per claim 18, Pontius and Miyamoto also teach that reading and writing are part of a FIFO process (Pontius; Col 4 Lines 37 – 46) (Miyamoto; Col 3 Lines 34 – 37).

As per claim 19, Pontius and Miyamoto also teach that the asynchronous memory is an asynchronous FIFO memory (Pontius; Col 4 Lines 37 – 46) (Miyamoto; Col 3 Lines 34 – 37).

(10) Response to Argument

Appellant's arguments filed 27 April 2007 have been fully considered but they are not persuasive.

I. CLAIMS 1 – 4, 12 AND 13

Applicant has failed to identify any limitation that is not met by one of the references.

In response to applicant's argument that the modification of Pontius by the teachings of Yi would render the invention of Pontius unsatisfactory for its intended purpose, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

The teachings of Pontius and Yi are both geared towards gray-code processing and thus when combined, teaches applicants claim language regarding a FIFO data structure combined with code sequence processing by removing mirrored codes. One of ordinary skill in the art would know how to modify the teachings of Pontius to include

the teachings of Yi. The motivation to combine Pontius with the teachings of Yi is set forth in Yi as allowing for a geometrically reduced storage requirement (Yi; Col 2 Lines 54 – 58) as it enables gray encoding and decoding of binary code sequences that are less than full length.

II. CLAIM 16

Applicant makes the same argument as presented with respect to claims 1 – 4, 12 and 13.

III. CLAIMS 23 AND 24

Applicant makes the same argument as presented with respect to claims 1 – 4, 12 and 13.

IV. CLAIMS 5 – 11, 14 AND 15

Applicant has failed to identify any limitation that is not met by one of the references.

The Examiner argues that the teachings of Pontius and Yi do not teach away from those of Miyamoto, but are merely ordinary engineering design considerations. The excess capacity and wastefulness of 2^N depth FIFOs is an ordinary consideration when trying to balance capacity, space, and cost in the design of a system. Therefore Pontius and Yi do not teach away from Miyamoto, and the combination of the three references is proper.

V. CLAIMS 17 – 19

Applicant makes the same argument as presented with respect to claims 5 – 11, 14 and 15.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,
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